1   1. A processor comprising:

2   Intel Architecture-32 (IA-32) instruction set decoding logic; and

3   an expanded logical register set, coupled to said IA-32 instruction set, said

4   expanded logical register set including more than eight logical registers of a first type.

1   2. The processor of claim 1, wherein said expanded logical register set includes up

2   to sixteen logical registers of a first type.

1   3. The processor of claim 1, wherein said expanded logical register set includes up

2   to thirty-two logical registers of a first type.

1   4. The processor of claim 1, wherein the more than eight logical registers of a first

2   type include more than eight logical general integer registers.

1   5. The processor of claim 1, wherein the more than eight logical registers of a first

2   type include more than eight logical MMX® technology registers.

1   6. The processor of claim 1, wherein the more than eight logical registers of a first

2   type include more than eight logical SIMD (single instruction multiple data) floating-

3   point registers.

1   7. The processor of claim 1, further comprising:

2   expanded register set decoding logic, coupled to said IA-32 instruction set

3   decoding logic, to determine that an instruction includes an at least four-bit register

4   identifier, the four-bit register identifier to specify one logical register of said expanded

5   logical register set.

1   8.   The processor of claim 7, wherein said expanded register set decoding logic is

2   to decode an at least four-bit register identifier.

1   9.   The processor of claim 8, wherein said expanded register set decoding logic is

2   to decode the at least four-bit register identifier based at least in part on at least four bits

3   of a scale index base (SIB) byte of the instruction.

1   10. The processor of claim 9, wherein said expanded register set decoding logic is

2   to decode the at least four bit register identifier based at least in part on at least one bit

3   of a scale field of the scale index base (SIB) byte of the instruction.

1   11. The processor of claim 7, wherein said expanded register set decoding logic is

2   to decode an at least five bit register identifier.

1   12. The processor of claim 11, said expanded register set decoding logic is to

2   decode the at least five bit register identifier based at least in part on five bits of a scale

3   index base (SIB) byte of the instruction.

1   13. The processor of claim 12, wherein said expanded register set decoding logic is

2   to decode the at least five-bit register identifier based at least in part on two bits of a

3   scale field of the scale index base (SIB) byte of the instruction.

1   14. A processor comprising:

2   decoder logic to decode Intel Architecture-32 (IA-32) instructions; and

3   means for decoding an instruction that specifies a logical register of an

4   expanded logical register set, the expanded logical register set including more than

5   eight logical registers.

1   15. The processor of claim 14, wherein said means for decoding includes means for

2   decoding an at least four-bit register identifier within the instruction.

1   16. The processor of claim 14, wherein said means for decoding includes means for

2   decoding the at least four-bit register identifier within the instruction based on at least

3   one bit within a scale field of a scale index base (SIB) byte of the instruction.

1   17. A method to access an expanded logical register set of a processor, the method

2   comprising:

3   determining that a mod field of a ModR/M byte of an Intel Architecture-32 (IA-

4   32) instruction contains a value selected from the values of 01B, 10B, and 00B;

5   determining that an r/m field of the ModR/M byte of the IA-32 instruction

6   contains a value of 100B;

7   determining that an index field of a scale index base (SIB) byte contains a value

8   of 100B; and

9   decoding an at least four-bit logical register identifier.

1   18. The method of claim 17, wherein decoding an at least four-bit logical register

2   identifier is based at least in part on at least one bit of a scale field of a scale index base

3   (SIB) byte of the IA-32 instruction.

1   19. The method of claim 17, wherein decoding an at least four-bit logical register

2   identifier includes decoding an at least five-bit logical register identifier.

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1   20. The method of claim 19, wherein decoding an at least five-bit logical register

2   identifier is based at least in part on two bits of a scale field of a scale index base (SIB)

3   byte of the IA-32 instruction.

1   21. A processor comprising:

2   a logical register set including more than eight logical registers of a first type;

3   instruction decoding logic coupled to the logical register set, said instruction

4   decoding logic including:

5   a first comparator to determine that a mod field comparator to a

6   ModR/M byte of an Intel Architecture-32 (IA-32) instruction contains a value

7   selected from the values of 01B, 10B, and 00B;

8   a second comparator to determine that an r/m field of the ModR/M byte

9   of the IA-32 instruction contains a value of 100B;

10   a third comparator to determine that an index field of a scale index base

11   (SIB) byte contains a value of 100B; and

12   a decoder to decode an at least four-bit logical register identifier.

1   22. The processor of claim 21, wherein the decoder to decode an at least four-bit

2   logical register identifier is to decode the at least four-bit logical register identifier

3   based at least in part on at least one bit of a scale field of a scale index base (SIB) byte

4   of the IA-32 instruction.

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